CLAIMS:

1. A $6F^2$ DRAM array including:

a first memory cell including a first access transistor and a first data storage capacitor, a first load electrode of the first access transistor being coupled to the first data storage capacitor via a first storage node formed on the substrate;

a second memory cell including a second access transistor and a second data storage capacitor, a first load electrode of the second access transistor being coupled to the second data storage capacitor via a second storage node formed on the substrate, the first and second access transistors each including a gate dielectric with a first thickness; and

an isolation gate formed between the first and second storage nodes and configured to provide electrical isolation therebetween, the isolation gate including an isolation gate dielectric with a second thickness that is greater than the first thickness used in at least the access transistors.

2. The $6F^2$ DRAM array of claim 1, wherein the second gate dielectric is formed by a deposition process in a shallow trench.

3. The $6F^2$ DRAM array of claim 1, wherein the second thickness is between thirty percent and seventy percent thicker than the first thickness.

4. The $6F^2$ DRAM array of claim 1, wherein the first thickness is about fifty Angstroms, and the second thickness is in a range of from about seventy Angstroms to about one hundred Angstroms.

5. The $6F^2$ DRAM array of claim 1, wherein the first and second gate dielectrics comprise silicon dioxide.

6. The $6F^2$ DRAM array of claim 1, wherein each of the access transistors includes a second load electrode coupled to a respective bitline contact, and wherein each of the access transistors has a threshold voltage determined in part by a halo implant on a bitline contact side only of the access transistor.

7. A DRAM array formed on a semiconductive substrate and including:

a first memory cell including a first access device and a first data storage capacitor, a first load electrode of the first access device being coupled to the first data storage capacitor via a first storage node formed on the substrate;

a second memory cell including a second access device and a second data storage capacitor, a first load electrode of the second access device being coupled to the second data storage capacitor via a second storage node formed on the substrate, the first and second access devices having a first threshold voltage; and

an isolation gate formed between the first and second storage nodes and configured to provide electrical isolation therebetween, the isolation gate having a second threshold voltage that is greater than the first threshold voltage.

8. The DRAM array of claim 7, wherein:

the first and second access devices each include a second load electrode coupled to a respective bitline, a gate coupled to a respective wordline and a gate dielectric separating the gate from the substrate, each gate dielectric having a first thickness; and

the isolation gate comprises a portion of an isolation device that includes a first load electrode corresponding to the first storage node, a second load electrode corresponding to the second storage node, a gate coupled to a voltage configured to turn the isolation device OFF and an isolation gate dielectric separating the gate from the substrate, the isolation gate dielectric having a second thickness greater than the first thickness.

9. The DRAM array of claim 7, wherein second load electrodes of the first and second access devices are coupled to bitline contacts and have been angle implanted.

10. The DRAM array of claim 7, wherein each of the first and second memory cells has an area of $6F^2$, wherein F is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus a width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array.

11. The DRAM array of claim 7, wherein the isolation gate comprises a portion of an isolation transistor that includes a first load electrode corresponding to the first storage node, a second load electrode corresponding to the second storage node, a gate coupled to a voltage configured to turn the isolation gate OFF and a gate dielectric separating the gate from the substrate, the gate dielectric being formed in a shallow trench.

12. The DRAM array of claim 7, the first and second access devices each include a second load electrode coupled to a respective bitline, a gate coupled to a respective wordline and a gate dielectric separating the gate from the substrate, each gate dielectric having a first thickness of about fifty Angstroms; and

the isolation gate comprises a portion of an isolation device that includes a first load electrode corresponding to the first storage node, a second load electrode corresponding to the second storage node, a gate coupled to a voltage configured to turn the isolation device OFF and an isolation gate dielectric separating the gate from the substrate, the isolation gate dielectric having a second thickness in a range of from about seventy Angstroms to about one hundred Angstroms.

13. A method of forming memory cells in a $6F^2$ DRAM array including:

forming a first memory cell including a first access transistor and a first data storage capacitor, a first load electrode of the first access transistor being coupled to the first data storage capacitor via a first storage node formed on the substrate;

forming a second memory cell including a second access transistor and a second data storage capacitor, a first load electrode of the second access transistor being coupled to the second data storage capacitor via a second storage node formed on the substrate, wherein forming the first and second memory cells includes forming the first and second access transistors to have gate dielectrics with a first thickness; and

forming an isolation gate between the first and second storage nodes and configured to provide electrical isolation therebetween, wherein forming the isolation gate includes forming an isolation gate dielectric to have a second thickness that is greater than the first thickness used in at least the first and second access transistors.

14. The method of claim 13, wherein forming an isolation gate dielectric comprises:

forming a shallow trench;

forming an isolation gate dielectric by a deposition process that fills the shallow trench with a dielectric material; and

planarizing the dielectric material using chemical-mechanical polishing.

15. The method of claim 14, further comprising implanting dopant into the shallow trench prior to forming an isolation gate dielectric.

16. The method of claim 13, wherein forming an isolation gate dielectric comprises forming the isolation gate dielectric to have the second thickness that is between thirty percent and seventy percent thicker than the first thickness.

17. The method of claim 13, wherein forming the first and second memory cells includes forming the first thickness to be about fifty Angstroms, and forming an isolation gate dielectric comprises forming the second thickness to be in a range of from about seventy Angstroms to about one hundred Angstroms.

18. The method of claim 13, wherein forming the first and second memory cells includes forming the first and second gate dielectrics to be silicon dioxide.

19. The method of claim 13, wherein forming the first and second memory cells includes:

forming each of the access transistors to include a second load electrode coupled to a respective bitline contact; and

implanting a halo implant in each of the access transistors bitline contact side only to provide a threshold voltage determined in part by the halo implant.

20. The method of claim 13, wherein:

forming first and second memory cells includes forming access transistors having a first threshold voltage having a first magnitude; and

forming an isolation gate includes forming the isolation gate to have a second threshold voltage having a magnitude greater than the first threshold voltage.

21. The method of claim 13, wherein forming an isolation gate comprises forming isolation gate between the first and second storage nodes and configured to provide electrical isolation therebetween by being biased to a negative potential, thus reducing subthreshold leakage by further reducing gate induced drain leakage.

22. A method of isolating a single row of memory cells in a $6F^2$ DRAM array comprising:

providing pairs of rows of memory cells, each row including a plurality of access devices each having a gate dielectric with a first thickness; and

providing an isolation gate separating rows comprising each pair of rows, each isolation gate having a gate dielectric with a second thickness, the second thickness being greater than the first thickness, the isolation gates being configured to isolate one of the pair of rows from another of the pair of rows in response to application of a suitable voltage.

23. The method of claim 22, wherein providing access devices in each of the rows comprises providing access devices having a threshold voltage determined in part by a halo implant on a bit contact side only of the access device.

24. The method of claim 22, wherein providing access devices in each of the rows comprises providing access devices having a gate dielectric comprising an oxide having a thickness of about fifty Angstroms.

25. The method of claim 22, wherein:

providing access devices in each of the rows comprises providing access devices having a first threshold voltage having a first magnitude; and

providing pairs of rows of memory cells comprises providing rows of memory cells, each pair of rows being separated by an isolation gate having a second threshold voltage having a magnitude greater than the first threshold voltage.

26. The method of claim 22, wherein providing an isolation gate comprises:

forming a shallow trench;

forming an initial dielectric filling the trench;

planarizing the initial dielectric to provide an isolation gate dielectric; and

forming a gate atop the isolation gate dielectric.

27. The method of claim 26, further comprising further comprising implanting dopant into the shallow trench prior to forming an initial dielectric.

28. The method of claim 22, wherein providing an isolation gate comprises:

forming an initial oxide via a thermal oxidation process;

stripping the initial oxide from areas that will become access devices; and

performing another thermal oxidation to provide isolation gate dielectric material having one thickness in isolation gate areas and to provide another gate dielectric material having another thickness that is less than the one thickness in access device gate areas.

29. The method of claim 22, wherein providing an isolation gate comprises providing an isolation gate configured to be coupled to a negative voltage, thus reducing subthreshold leakage by further reducing gate induced drain leakage.